
Chapter 9

The Bus Error Circuit

The Bus Error circuit is somewhat unique to the 68000. It acts much like automobile insurance - It is there in case of problem, but hopefully you will not need it.

9-1. Discussion

Each time the 68000 wants to access memory or I/O, it sends out the address, $\overline{\text{LDS}}$ and/or $\overline{\text{UDS}}$, $\text{R}/\overline{\text{W}}$, and $\overline{\text{AS}}$. Then it sits back and waits for the external circuitry to respond. If all goes well, the external circuits are supposed to return a low on $\overline{\text{DTACK}}$ (data transfer acknowledge); if something goes wrong, they are supposed to return a low on $\overline{\text{BERR}}$ (bus error).

The $\overline{\text{DTACK}}$ signal is supposed to tell the 68000 how fast it can go; slow memory or I/O tells the 68000 to slow down and insert wait states. But suppose the 68000 program accidentally calls some address at which there is no memory or I/O - what then? Since there is nothing to generate a $\overline{\text{DTACK}}$ signal, the 68000 might sit there forever, waiting. That's where the bus error circuit comes in - its job is to detect the lack of $\overline{\text{DTACK}}$ after some time and generate $\overline{\text{BERR}}$, which then sends the 68000 into an error recovery procedure.

When we first powered up the 68000 in Chapter 7, we forced $\overline{\text{DTACK}}$ to be low and forced $\overline{\text{BERR}}$ to be high. This forced the processor to go at its maximum speed, and made sure that a bus error would never occur. Since we are still providing a fake $\overline{\text{DTACK}}$, the 68000 will go ahead even though there is no memory in the system yet, so we might as well put in the correct $\overline{\text{BERR}}$ circuit at this time.

Though the circuit in Fig. 9-1 looks complex, actually it consists of just two parts - U65, a 74LS390 dual decade counter, and U76, a 74LS175 quad D flip-flop.

U76 74LS175 quad D flip-flop and its socket.

(U66f has been installed previously.)

9-2a. Additional Construction Step

If you have a very early SK68K printed circuit board, then your circuit board contains an error, for which we apologize. On your board, the clock input to pin 9 of U76 (shown in Fig. 9-1) goes to the E output from the 68000, instead of going to U65 as shown in the diagram. This earlier connection works well with older XT-compatible boards, but does not work with some of the newer video boards.

To make the change, please cut the trace from U76-9 to U47-20, and install a jumper from U76-9 to U65-10.

9-3. Testing

Using the LED probe, look at pins 4 and 9 of U76. Since \overline{AS} and the 80 kHz clock pulses are both pulses, the LED will glow but only dimly. Then look at pin 2, the Q output of the first flip-flop. Since \overline{AS} and the 80 kHz signal are not in any particular phase relationship - one is at 1 MHz while the other runs at 80 kHz - the first flip-flop will trigger once every few \overline{AS} cycles, but never stay on very long. Thus the flip-flop is mostly off, and the LED should be quite dim. In normal operation, the other flip-flops never get a chance to set, and so the LED should stay dark when testing any of the other Q outputs. BERR, of course, is a high all the time, so the LED should be bright when testing pin 14.

